rm 1449A/PTO (Modified) many sheets as necessary)	Attorney Docket No.: 42390.P9429	Application Number: 09/608,637
Sheet 1 of 1	First Named Inventor: Jin Yang	Examiner: Unassigned
	Filing Date: June 30, 2000	Art Unit: 2763

OTHER ART – NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation[2]
/DC/		BRADLEY, J., et al., "Compositional BDD Construction: A Lazy Algorithm," Department of Computer Science, University of Bristol, UK, April 6, 1998	
/DC/		BURCH, E. M., et al., "Symbolic Model Checking for Sequential Circuit Verification," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 13, Issue 4, April 1994, pp. 401-424	
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/DC/		ZHANG, ZHANG, "An Apprpoach to Hierarchy Model Checking via Evaluating CTL Hierarchically," Proceedings of the Fourth Asian Test Symposium, 1995 – Bangalore, India, November 1995, pp. 45-49	

Examiner Signature	/Dwin Craig/ (10/15/2007)	Date Considered	

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[1]Unique citation designation number. [2]Applicant is to place a check mark here if English language Translation is attached.